Compact Broadband Microstrip Patch Antenna with Chip Resistor Loading

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Abstract

Microstrip antenna loaded with shorting pin for reducing size is well known area of research. Recently it has been proposed that by replacing the shorting pin with a chip resistor of low resistance value, the required antenna size can be significantly reduced for the same antenna operating at a high frequency. Moreover the antenna bandwidth is also enhanced. To demonstrate the capability of such a chip-resistor loading technique, related design for a rectangular microstrip antenna has been studied.

In this paper the design of chip-resistor-loaded rectangular microstrip patch antenna with probe-feed is presented. These antenna designs have the advantages of small antenna size and wide impedance bandwidth, compared to a conventional rectangular patch antenna.

The proposed antenna is simulated using computer simulation technology (CST) Microwave Studio. The simulated results show that the proposed antenna resonates at 897.48 MHz, which is much lower than that of (2.4448 GHz) conventional patch antenna; moreover the -10 dB return loss impedance bandwidth is 7.6%, about 4.9 times that (1.4%) of a conventional patch antenna. This suggests that antenna size reduction can be greater by using a chip resistor.

Key words: Microstrip Patch Antenna, Impedance Bandwidth, CST Microwave Studio.

• Introduction

Conventional microstrip antennas in general have a conducting patch printed on a grounded microwave substrate, and have the attractive features of low profile, light weight, easy fabrication, and conformability to mounting hosts [1]. However, microstrip antennas inherently have a narrow bandwidth, and bandwidth enhancement

is usually demanded for practical applications. In addition, applications in present-day mobile communication systems usually require smaller antenna size in order to meet the miniaturization requirements of mobile units. Thus, size reduction is becoming major design considerations for practical applications of microstrip antennas.

In recent years, the demand for broadband antennas have increased for use in high-frequency and high-speed data communication systems. Printed antennas are economical and easily hidden inside packages, making them well suited for consumer applications. Unfortunately, a "classical" microstrip patch antenna has a very narrow frequency bandwidth that precludes its use in typical communication systems. However, if the frequency bandwidth could be widened, a broad-band microstrip antenna would prove very useful in commercial applications such as 2.5 G and 3 G wireless systems, wireless local area networks (WLAN), and Bluetooth personal networks. For these reasons, studies to achieve compact and broadband operations of microstrip antennas have greatly increased.

Researchers have devised several methods to increase the bandwidth of microstrip antennas in addition to the common techniques of increasing patch height and decreasing substrate permittivity [6, 7]. These include using a multilayer structure consisting of several parasitic radiating elements with slightly different sizes above the driven element (a stacked patch antenna) [2] or a planar patch antenna surrounded by closely spaced parasitic patches (a coplanar parasitic sub array) [3, 4]. The stacked patch antenna increases the thickness of the antenna while the coplanar geometry increases the lateral size of the antenna.

It has been pointed out by the Pozar [5], the impedance bandwidth of patch antenna can be increased by introducing losses in the antenna. The losses can be in the form of lossy substrate materials, layer of lossy film, or a discrete chip resistor. So in this paper a chip-resistor-loaded patch antenna is presented and designed using CST Microwave Studio. The proposed patch antenna resonates at 897.48 MHz and exhibits -30.5dB return loss at this resonating frequency. The same patch antenna without using resistance (conventional antenna) resonates at 2.4448GHz frequency. In this way, with the same antenna parameters the obtained antenna size reduction can be greater than for the design using chip-resistor loading. Moreover, the obtained impedance bandwidth can be increased as compared to conventional patch antenna.

Antenna Configuration

In this paper, the geometry of a probe-fed rectangular microstrip patch antenna with and without chip-resistor loading given in Figure 1 is studied. The rectangular patch had dimensions $L \times W$, and the substrate has a relative permittivity of ε_r and thickness h. A 1 Ω resistance was selected and placed at about the edge of the patch (d_c=1mm) for maximum resonant frequency reduction. The patch antenna is fed by the co-axial probe of 50 Ω . We first analyze the behaviour of chip-resistor-loaded rectangular patch antenna and then compare its behaviour with conventional rectangular patch antenna. The substrate has dimensions $L_g \times W_g$. The geometric and material parameters for the proposed antenna are given in Table 1. The dimensions of the patch antenna are given in mm.

d _c 1	d _p L ₂ 7.33 41	W _g 36			
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		$ \begin{array}{c} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	L		→ x
	chip resi	stor	prot	be	
	[׺	ε _r	substrate	th
		Fig	gure 1(a)		

Table 1 Dimension and Material Properties of Chip-Resistor Loaded Patch Antenna



Figure 1 (a): Geometry of Chip Resistor Loaded Patch Antenna

W

22

28

Н

1.6

ε_r

4.4

(b): Structural View of Chip-Resistor-Loaded Patch Antenna

We conducted a parametric study on the above structure by changing the parameter dc (location of chip resistor). The figure 2 shows that how return Loss and resonant frequency varies with the location of resistance (d_c) along the x axis.



Figure 2: Effect of Resistance Location

d _c	Resonant frequency (f _r)	S ₁₁
0.5mm	876.45 MHz	-21.5 dB
1.0mm	897.48 MHz	-30.5 dB
1.5mm	918.51 MHz	-30.5 dB

Table 2 Effect of resistance location

A chip resistor of 1Ω is selected in this study and is placed at the edge of the patch (d_c) for maximum resonant frequency reduction. The resistance position designated by d_c is varied from 0.5 to 1.5 mm. From the Table 2 we can conclude that the optimum value of d_c for better response of proposed antenna is 1 mm.

• Result and Discussion

The proposed patch antenna is simulated using CST Microwave Studio. The result of the simulated return loss against frequency for chip-resistor-loaded patch with impedance matching is shown in figure 3. It can be observed that the resonant frequency is about 897.48 MHz and the bandwidth that determined from the -10 dB return loss is 7.6%. For the purpose of comparison, an antenna using the same size and substrate but without chip resistor is also analysed and its return loss verses frequency plot is shown in figure 3(b). It is observed that conventional patch antenna is resonating at about 2.4448 GHz and -10dB bandwidth is about 1.4% around the centre frequency. Table 3 compares the resonant frequency (f_r) and the return loss (S_{11}) of the proposed antenna with a conventional patch antenna (without chip resistance).

Table 3 Comparing Unip-Resistor- Loaded Patch Antenna with Conventional Ant

Antenna	$f_{r}\left(GHz\right)$	S ₁₁ (dB)	Impedance Bandwidth
Conventional	2.4448	27.7	1.4%
Resistance loaded	0.8974	30.5	7.6%





Figure 3(b)

Figure 3(a): Return loss Vs Frequency Plot for chip-resistor-loaded patch antenna. 3(b): Return Loss Vs Frequency Plot for Conventional Patch Antenna.

The simulated input impedance of the proposed antenna is shown in figure 4. This plot shows that how the antenna impedance varies with frequency.



Figure 4(a): Smith Chart For Chip-Resistor-Loaded Patch Antenna.

4(b): Smith Chart for Conversional Patch Antenna.

Conclusion

A chip-resistor-loaded patch antenna has been designed and simulated using Computer Simulation Technology (CST) Microwave Studio Software. This proposed antenna is resonates at 897.48 MHz, which is much lower than that of (2.4448 GHz) conventional patch antenna; moreover the -10 dB return loss impedance bandwidth is 7.6%, about 4.9 times that (1.4%) of a conventional patch antenna. This suggests that antenna size reduction can be greater by using a chip resistor.

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